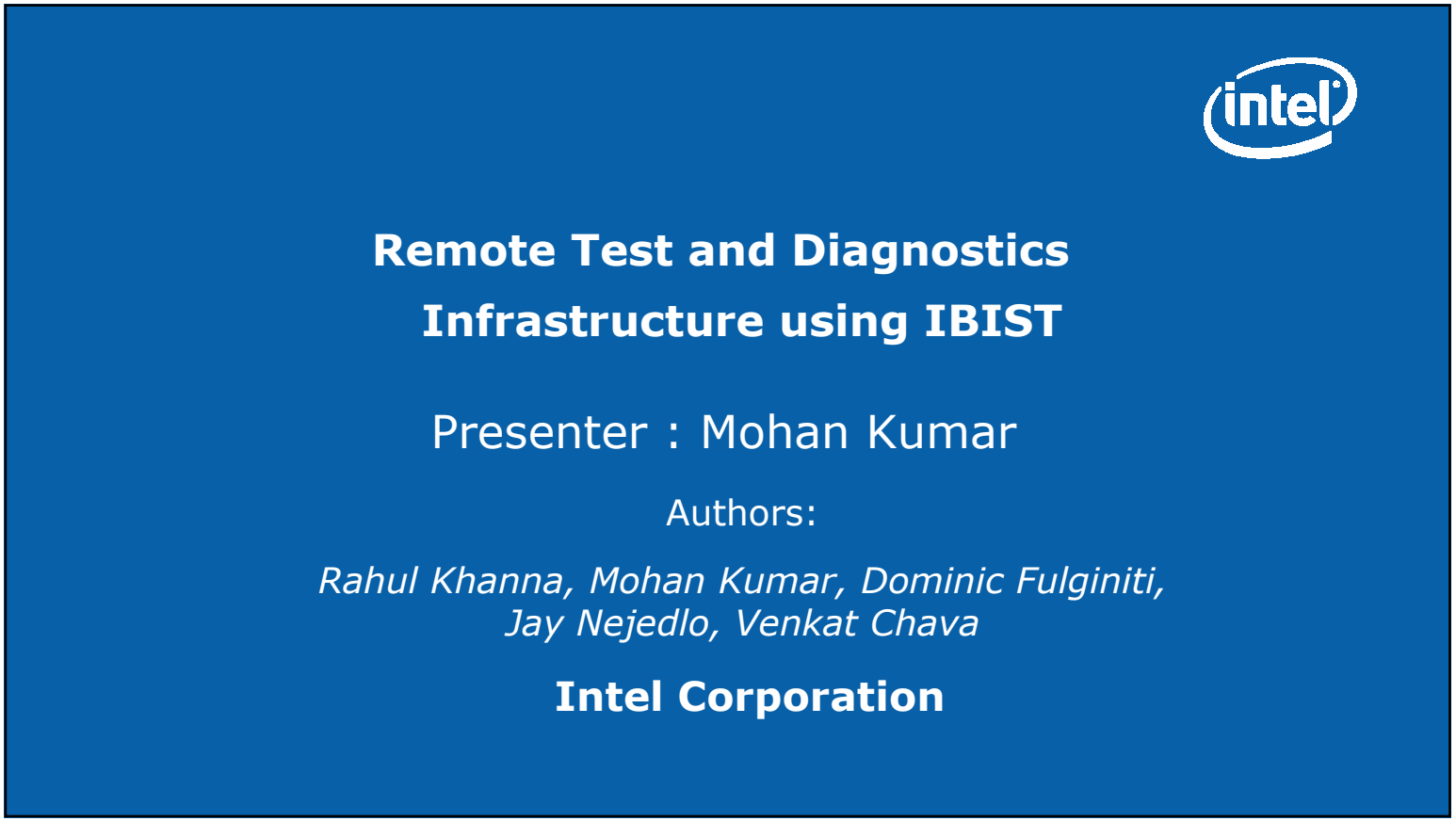

Remote Test and Diagnostics
Infrastructure using IBIST
Presenter : Mohan Kumar
Authors:
Rahul Khanna, Mohan Kumar, Dominic Fulginiti,
Jay Nejedlo, Venkat Chava
Intel Corporation

Outline

- Motivation
- Advantages of IBIST
- Modular Software Strategy
- Logical Architecture
- Diagnostics Hardware Abstractions (DHA)
- Standards-Based Remote Diagnostics

Motivation: Next Generation Test Challenges

PCB routing densities, reduced timing budgets

- Physical access → In-circuit test …. is dead!

Performance levels

- Higher operating frequencies
  - Oscilloscope resolution not keeping pace
  - (can't differentiate goodness vs. badness)
- IO filtering techniques
  - Using techniques like "equalization" means we can't externally detect an eye (pad or pins) →Means "scrap traditional validation techniques" (scopes & probes)

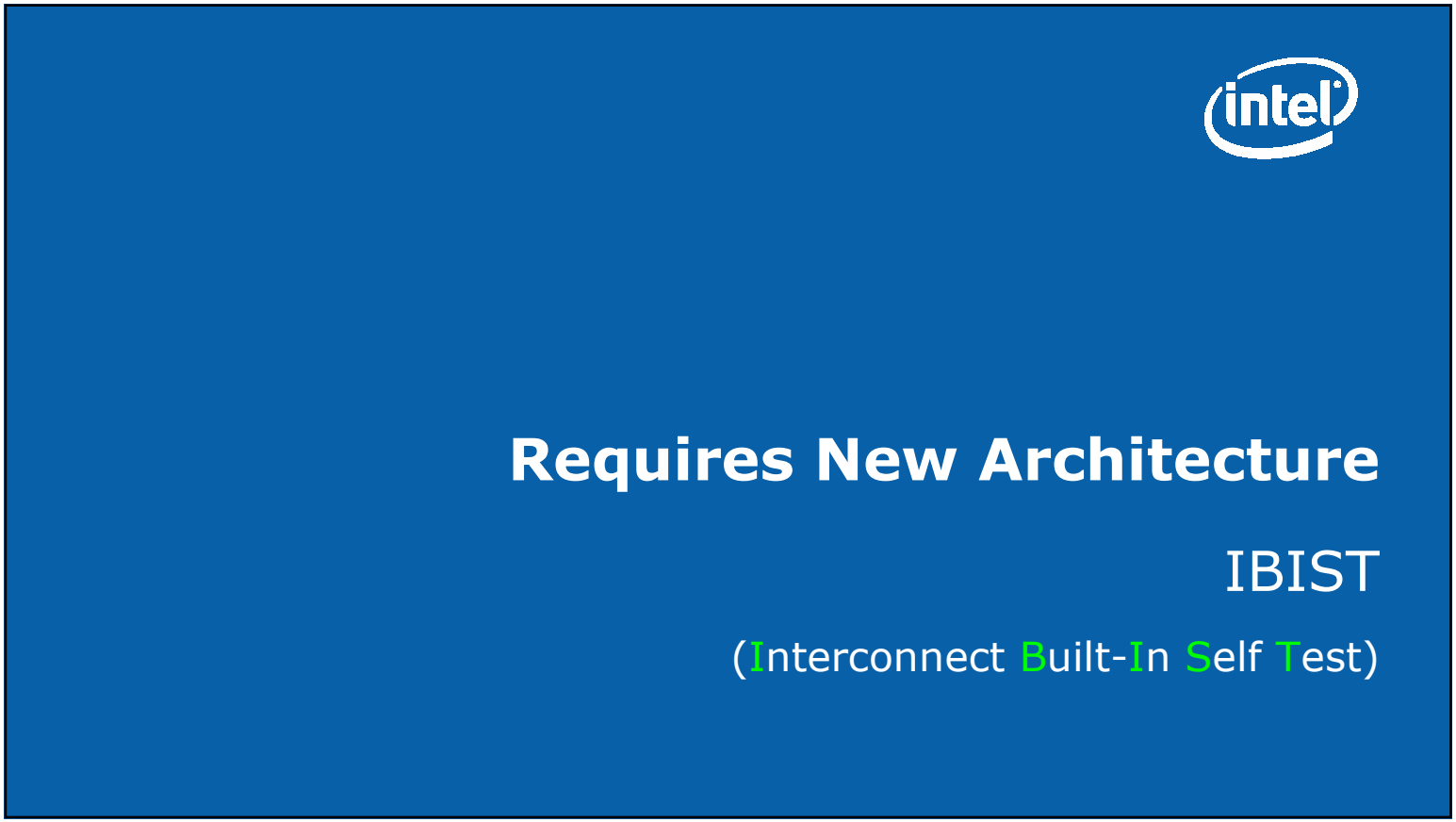
Motivation: Next Generation Test Challenges

Power density

- Ensure current source/sink ability of BGA power and ground Quality & Reliability

Quality & reliability

- High speed bus interconnect integrity
- Verify meeting of BER specification of interface
- Cost (design validation and factory test time)
- Platform complexity/diversity requires a re-think of traditional test techniques


Requires New Architecture
IBIST
(Interconnect Built-In Self Test)

What is IBIST?

An on-die feature enabling board/system testing which addresses static and high frequency fault spectrum associated with high performance IO

- Facilitates the validation & testing of primary buses & interfaces

IBIST Test Usage

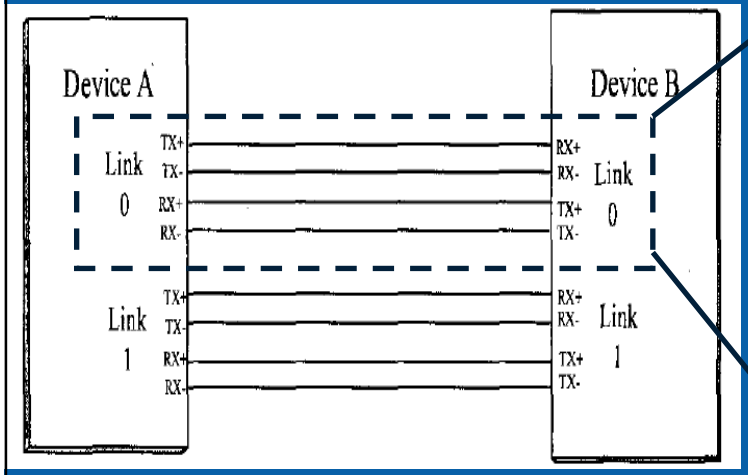
- AC Parametric & Stress Testing, Design Verification & High Volume Manufacturing
- System Performance Bus Characterization
- Assembly & Electrical Defect Detection, Board/Platform Debug, Platform Test
- Analog/Electrical Stress/Characterization & Debug

IBIST Benefits

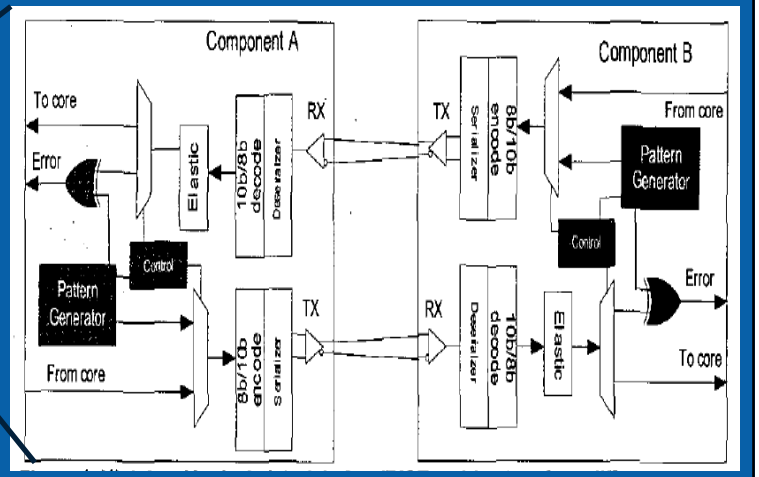
- Restores test access on all major buses through virtual nodal access
- Addresses expanded interconnect fault spectrum through advanced test pattern algorithms. Stresses all bus signals (data, address and control)
- Because IBIST operates independently of normal silicon operation and bus protocols enables testing to be completely deterministic.
- Auto-diagnosability, fault isolation/characterization (pin and pattern)

Nejedlo, J.J., "IBIST/spl trade/ (interconnect built-in-self-test) architecture and methodology for PCI Express," *ITC 2003*

IBIST Example



PCI Express x2 Lane Interconnection



High level IBIST Architecture for
High serial interconnect (per each link)

Papers

Nejedlo, J.J., "IBIST/spl trade/ (interconnect built-in-self-test) architecture and methodology for PCI Express," *Test Conference, 2003. Proceedings. ITC 2003. International* , vol.2, no., pp. 114-122 Vol.2, 30 Sept.-2 Oct. 2003

Nejedlo, J.J., "Tribute board and platform test methodology: Intel's next generation test and validation methodology for platforms," *Test Conference, 2003. Proceedings. ITC 2003. International* , vol.1, no., pp. 783-783, Sept. 30-Oct. 2, 2003

Nejedlo, J.J., "Functional test coverage effectiveness on the decline," *Test Conference, 2004. Proceedings. ITC 2004. International* , vol., no., pp. 1424-, 26-28 Oct. 2004

Eric Johnson, "Structural Testing of High-Speed Serial Buses: A Case Study Analysis," *Test Conference, 2006. ITC '06. IEEE International* , vol., no., pp.1-9, Oct. 2006

http://www.intertesttech.com/ate/company_news_ibist.htm

Advantages

- Enables the Diagnostics Infrastructure that can discriminate an Interconnect Error from a Component Error
  - Reduces NDF (No Defect Found)
- Enables the infrastructure to re-margin the interconnects due to environmental conditions
  - Temperature, Moisture
- Enables the infrastructure that can identify the interconnect de-gradation due to
  - Micro-cracks, Ageing, Dry-Solder, Temperature
- Enables the infrastructure that can evaluate the fault conditions in the customer environment.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How do we enable Eco-System
Software Strategy

Modular Software Strategy

Achieving Technology Goals
- Advancements toward faster product cycle times
- Increased quality requirements (through more advanced, more reusable tests)

Employing Advanced Software Techniques
- Standard IBIST Registers for all HW to follow
- Standard Diagnostics HW Abstractions (DHA) for sys SW
- Standard Remote Abstractions End-to-End model (CDM)

Serving Varied Usage Environments
- Design validation (post power on) internal & OEM
- High volume manufacturing (HVM)
- Aftermarket usage in the field

Modular Software strategy drives value through benefits reaching out to customers

Advantages

(1st level) Standardization of IBIST Registers

- Auto Discovery, code maturity, binding agreement b/w HW and system SW

(2nd level) Standardization of Diagnostic HW Abstractions (DHA)

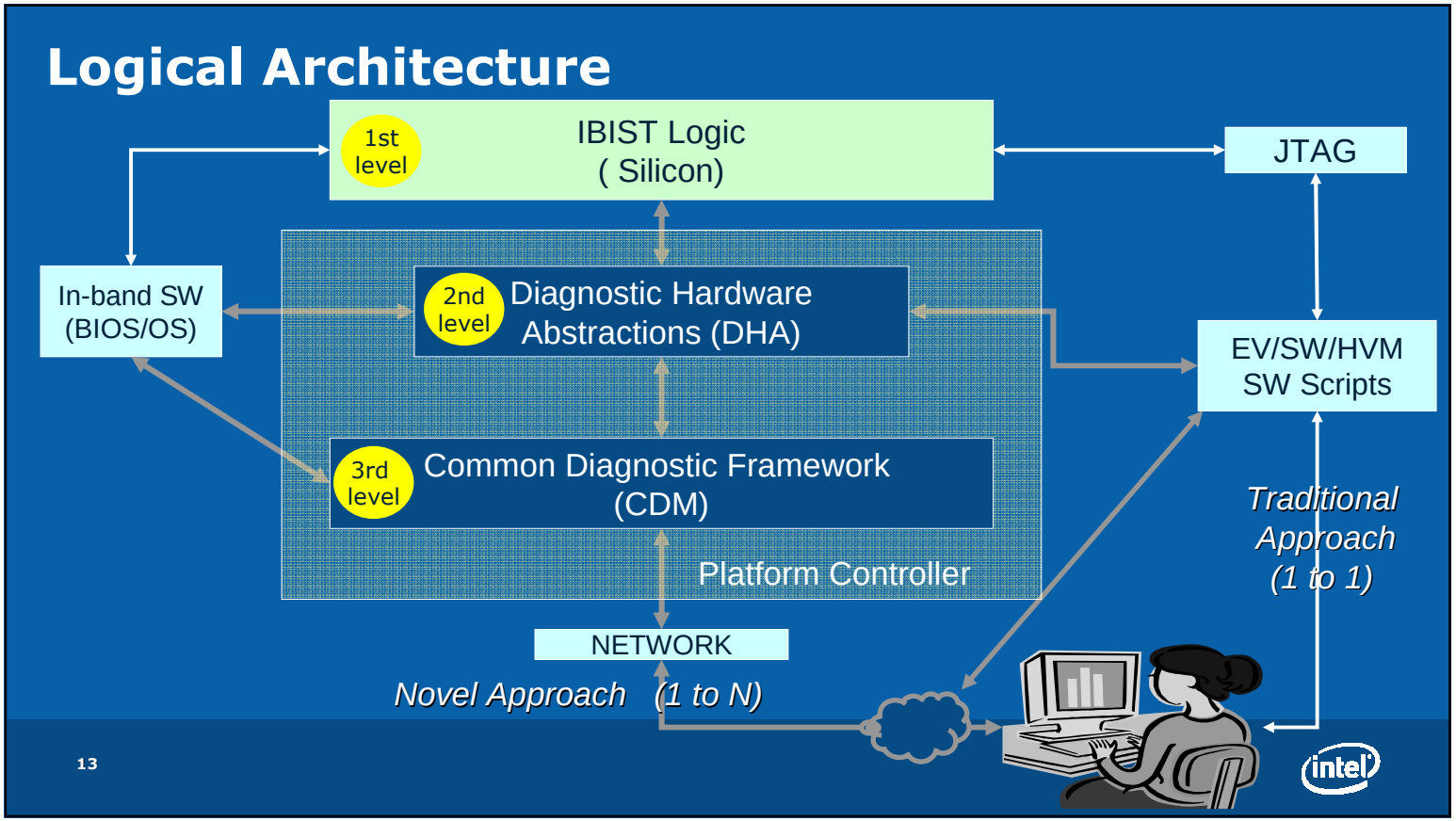
- Hides implementation details, utilized by multiple agents, isolates IP
- Enables Software Reuse (e.g. EV, DV, Firmware, BIOS)

(3rd level) Standardization of Remote Abstractions

- Centralized control, distributed correlation, using variable parameters
- Remote diagnosis at the customer environment
- Validation of multiple systems (under test) w/o specialized cabling

Multi-layered approach minimizes work throughout Platform Life Cycle

Logical Architecture



Diagnostic Hardware Abstractions (1)

Loopback and Compliance Abstractions

- Perform complex coordinated tests across lanes simultaneously

Pattern Generation Abstractions

- Flexible & programmable pattern generation and error checking

Pattern Checker Abstractions

- Programmable start bit & checking interval, flex checking specific bits

Error Counters Abstractions

- Records & retrieves error-log during a controlled data transmission and checking environment (Loopback)

Diagnostic Hardware Abstractions (2)

Parameter Setting Abstraction

- Compensation controls ICOMP, RCOMP
- Equalization settings for driver
- voltage (VOC) and timing (PI) offsets

BER Eye Diagram Abstraction

- Ratio of bits incorrectly received to total bits sent across the link
- By varying TX timing (PI) and voltage (VOC)

On Die Oscilloscope Abstractions

- Waveform capture w/ programmed pattern for a repetitive waveform

2nd level abstractions provide robust functionality and ease of reuse

Standards-based Remote Diagnostics

A Suite of standards

purpose-built

by the industry-recognized Distributed Management Task Force (DMTF)

enabling and end-to-end platform solution

CDM

Common Diagnostics Model

SM CLP

Server Management Command Line Protocol

MCTP

Management Controller Transport Protocol

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Standards-based Remote Diagnostics – CDM (1)

Rules for representation - uses Common Information Model (CIM)

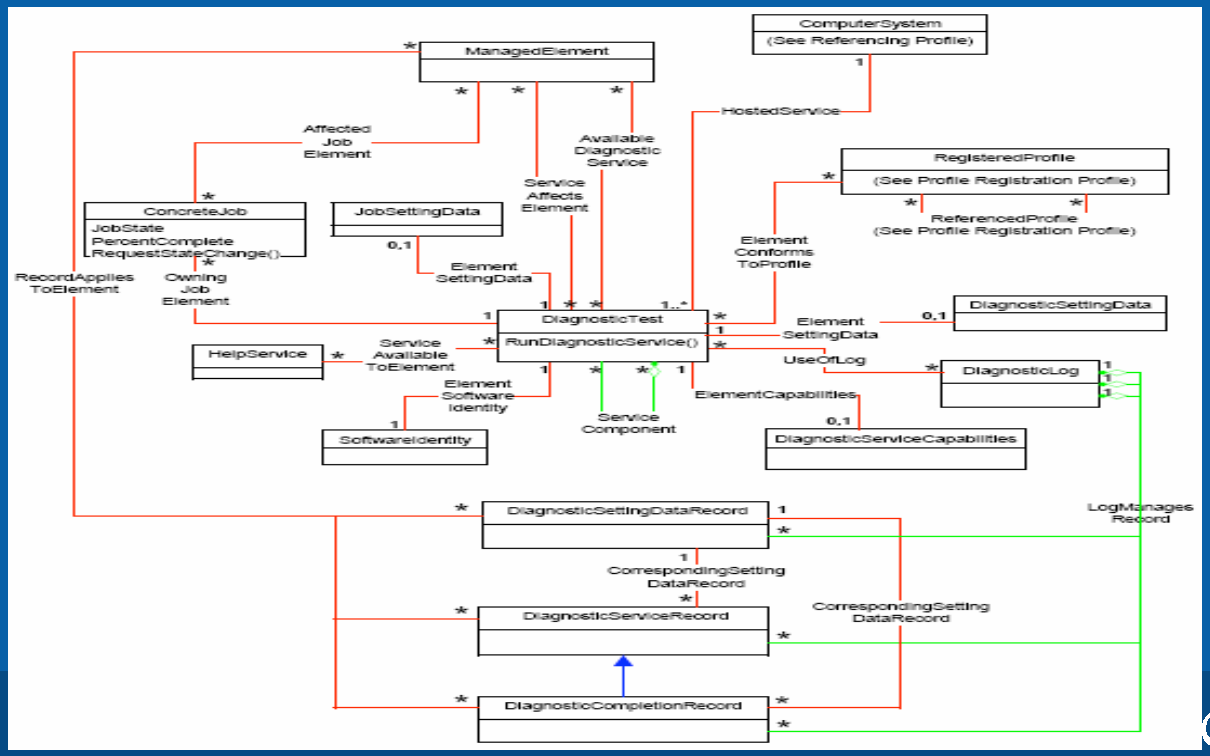
- Classes, Instances, Attributes, Methods, Associations (i.e. object oriented)
- Expressiveness in describing test attributes
  - Safety, exclusivity, relation to devices
- Associated constructs for runtime management
  - Running jobs, logged results

Standard way to describe & discover diagnostics

- Major Si vendors, OEMs, SW Vendors committed to CDM
- Many delivering compliant devices/drivers
- Can work in-band and out-of-band

CDM provides highly flexible model for representing diagnostics

Standards-based Remote Diagnostics – CDM (2)



Standards-based Remote Diagnostics - SM CLP

Industry Adoption

- Showing up in many layers of server platforms & infrastructure
  - BMCs, mgmt cards, rack aggregators, OS services
- Applicable to other platforms as well (comms, desktop, mobile, etc.)
- Not the only remote protocol allowing access to CIM-based services
  - WS-Management present in newest client mgmt standards and AMT
  - WMI/scripting for in-band

Simple Scriptable and Interactive Experience

- Allows rapid productivity and reuse with minimal client setup cost/complexity
- All you need is a remote shell, such as Secure Shell Host (SSH)

Dynamic

- Together with CIM/CDM, allows remote discovery of platform specific diagnostics

Standards-based Remote Diagnostics - MCTP

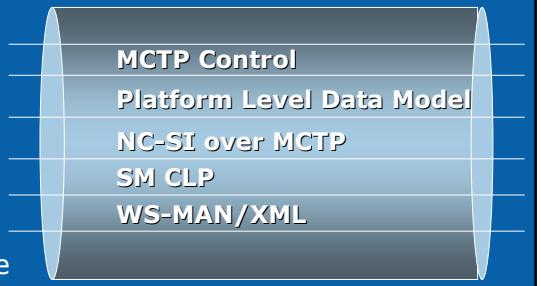
Management **C**omponent **T**ransport **P**rotocol

- For 'inside the box' communication of platform management traffic between mgmt devices
- Multiple message types for mgmt bus sharing
- Multiple media types (SMBus, PCIe and more)
- Suitable to server, desktop, mobile, comms
- Designed for low-cost microcontrollers

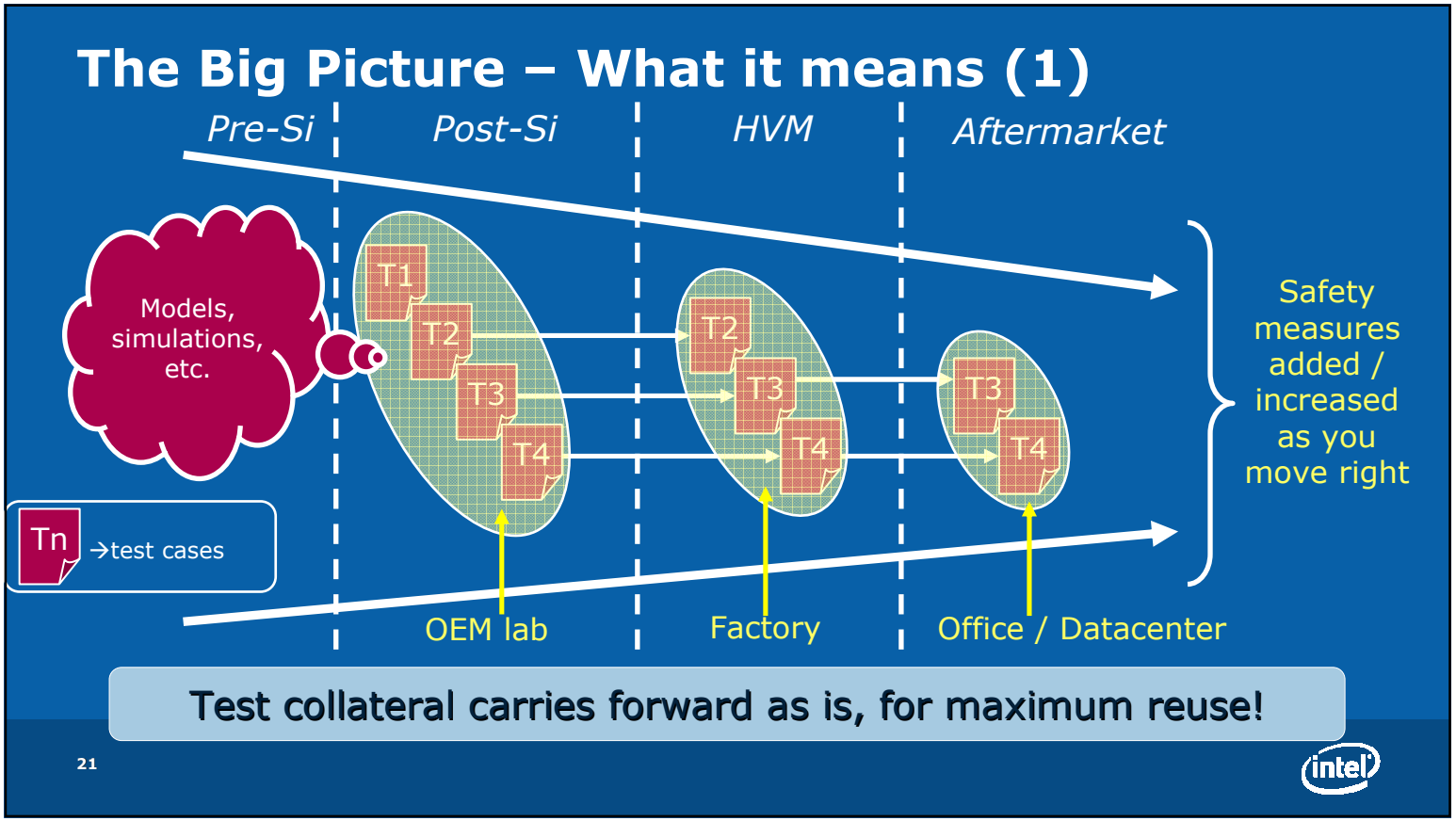
Platform Level Data Model

- Efficient low-level monitoring & control
  - Temp, fan, voltage, event logging, boot control, etc.
- Defines data rep & cmds to abstract the platform mgmt hardware
- Designed for effective mapping under CIM

Multiple message types on common transport



E2E solution standards span the platform – HW, FW, OEM, OSV/ISV


The Big Picture – What it means (1)
Pre-Si
Post-Si
HVM
Aftermarket
Models, simulations, etc.
T1
T2
T3
T4
T2
T3
T4
T3
T4
Safety measures added / increased as you move right
Tn
→test cases
OEM lab
Factory
Office / Datacenter
Test collateral carries forward as is, for maximum reuse!
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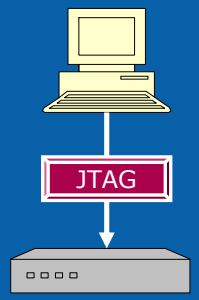
The Big Picture – What it means (2)

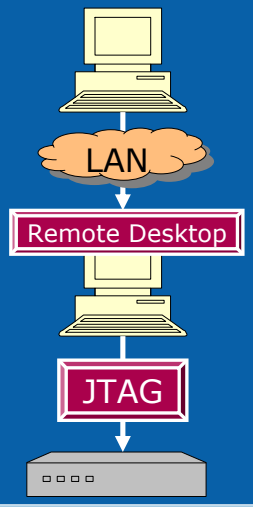
Old Way (OK)

1:1 – Local only



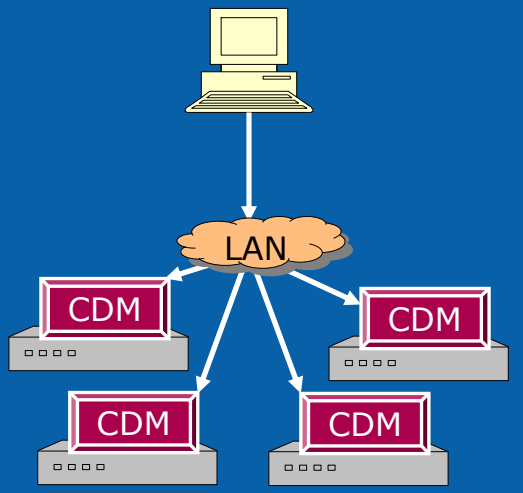
Old Way (Better)

1:1 – no travel ☺



Innovative Approach

1 to many, 1 to any! ☺☺



Enabling very powerful usage models/environments!

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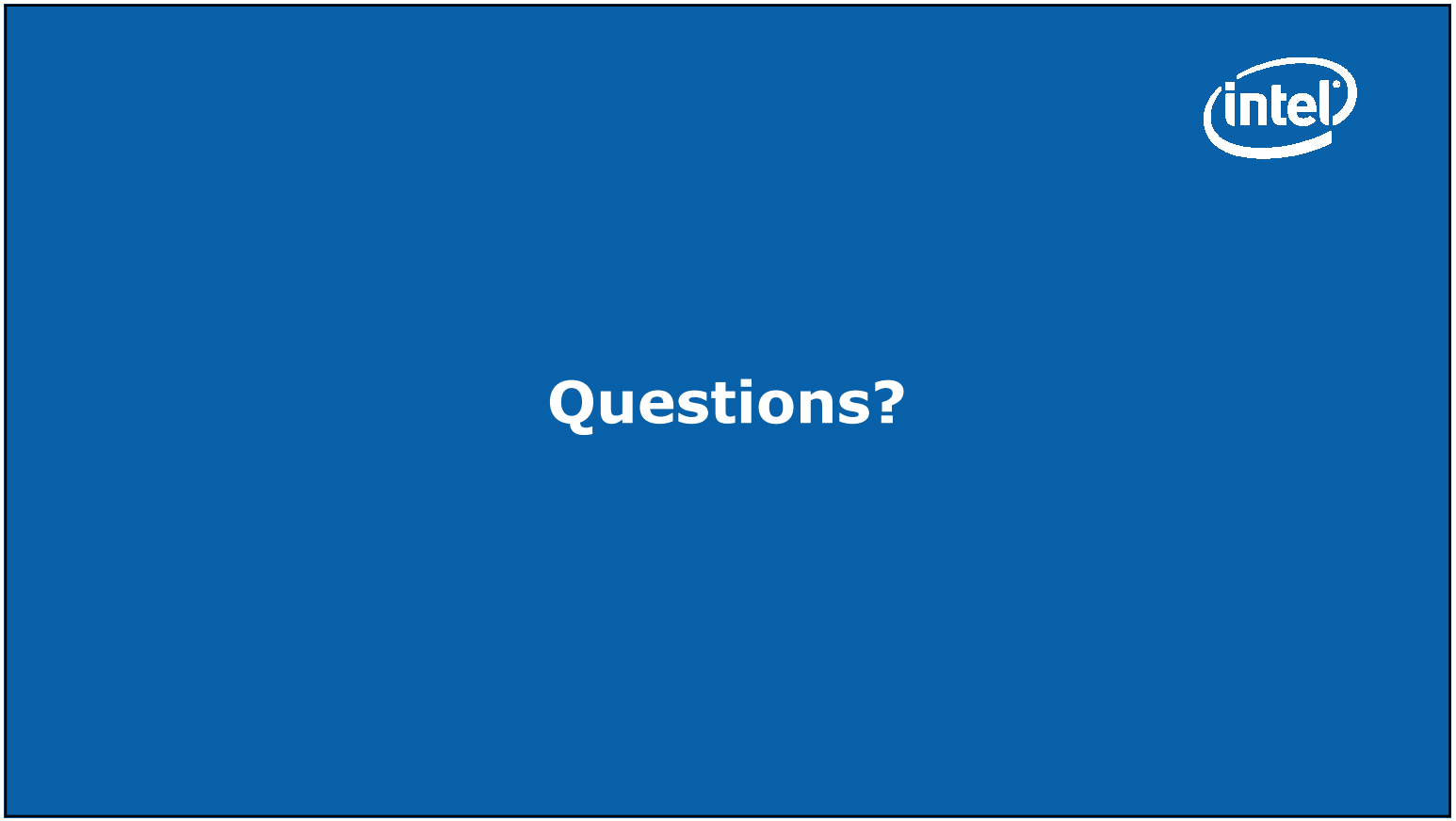
Conclusions

- Proposed diagnostic architecture allows test reuse across design, factory and field testing
- Benefits HVM by reducing test cost, greater test automation and multicast testing
- CDM provides highly flexible model for representing diagnostics
- E2E solution standards span the platform – HW, FW, OEM, OSV/ISV
- DMTF standards based approach allows abstraction of hardware implementation and IP
- Multi-layered approach minimizes work throughout Platform Life Cycle.
- Enables very powerful future usage models/environments!
  - Predictive Failure solutions
  - dynamic re-margining to extend RAS


Questions?